ICP Etch Processes for Nano-imprint Lithography

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In this paper the application of inductively coupled plasma (ICP) etching processes to three critical steps in the nanoimprint lithography (NIL) fabrication sequence is demonstrated. ICP etching gives excellent results which meet the stringent demands of NIL technology.

Introduction

Nanoimprint lithography (NIL) is a versatile, cost effective, flexible and high throughput method for fabrication of down to and below 10 nm structures [1] with a wide range of application within e.g. storage [2], optics [3] and bio-sensors [4]. The basic NIL sequence is illustrated in Figure 1 whereby the inverse of a stamp pattern is transferred into a polymer on a substrate and subsequently transferred into the substrate by dry etching.

Etching by low pressure of inductively coupled plasma (ICP) is a familiar means of patterning now being increasingly used for high quality patterning for nanoscale devices. The high ion density, low pressure ICP etch regime provides excellent control over etched profiles and critical dimension (CD) [5]. ICP may be used in three of the critical steps in the NIL sequence (Figure 1) A. Etching of the stamp D. Descum of the polymer residual and E. Patterning of the substrate. The suitability of ICP for these three steps is shown in this paper.

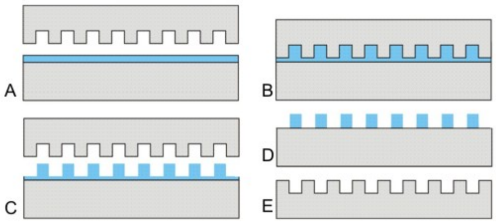

Figure 1. Schematic of the NIL process.
A. A stamp is fabricated in typically silicon or fused silica by electron beam lithography (EBL) and dry etching. B. The stamp is pressed into a soft thermoplastic, thermosetting or UV-curable polymer on a substrate combined with heating or UV radiation C Polymer cured and stamp released from substrate D. Residual imprint polymer under stamp protrusions removed by 'descum' process E. Imprinted pattern transferred into substrate by dry etching.

Experimental

Samples for fabrication of UV NIL stamps have been provided by NIL Technology, *www.nilt.com*. 500 µm thick fused silica wafers were prepared with 40 nm sputtered chromium (Cr) and 120 nm ZEP520A [6] high resolution positive resist by spin coating. The stamp pattern with down to 30 nm structures was defined by 100 kV EBL (Jeol JBX9300FS), dose 220 µC/cm^2, and developed for 2 min in ZEP-N50 [6].

Etching has been carried out in an Oxford Instruments Plasmalab System 100 ICP tool. This features a cylindrical ICP source, independent substrate electrode bias and wide electrode temperature capability [5].

Results and discussion

Stamp etch

The NIL process must replicate the structures on the stamp perfectly into the polymer. Thus, the stamp etch has demanding specifications regarding sidewall smoothness and angle, etched protrusion height uniformity and CD control. Ideally the stamp should have a vertical or very slightly tapered sidewall. A re-entrant or trenched profile is undesirable.

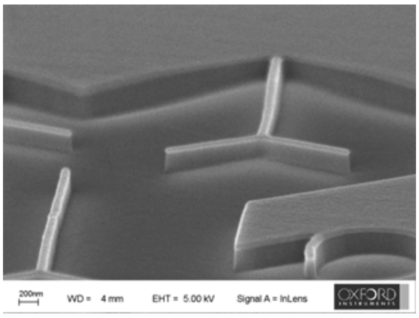

Figure 2. SEM image of optimized fused silica stamp etch (30nm features to 200nm depth)

An octofluorocyclobutane (C_4F_8)-oxygen (O_2) mixture was used for ICP etching of fused silica. Figure 2 shows an optimized stamp etch. 30nm features have been etched to 200nm depth at a uniform rate of 85nm/min with selectivity over a Cr mask >200:1. The profile is vertical and trench free. Figure 3 shows profile control by temperature. Trenching is an effect often seen for ion-driven processes such as silica etching and is manifested as deeper etching at the base of the sidewalls. Figure 3 also shows how trenching may be eliminated by reducing DC bias. ICP has the benefit of DC bias control largely independent of the other process parameters.

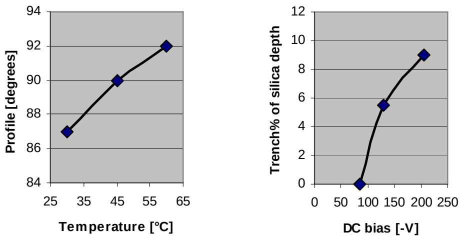

Figure 3. Control of profile (left) and trenching (right) for fused silica stamp ICP etch.

Descum

After imprinting there is inevitably some residual polymer under the stamp protrusions, typically 10-20 nm thick for stamp protrusion heights of 100-200 nm. Before final pattern transfer this residual must be removed with uniform and minimized CD and profile change of the features. ICP processing succeeds by enabling stable low pressure and hence anisotropic conditions. Cooling of the substrate also improves anisotropy. Figure 4 shows a good descum of a polystyrene residual (25% of protrusion height).

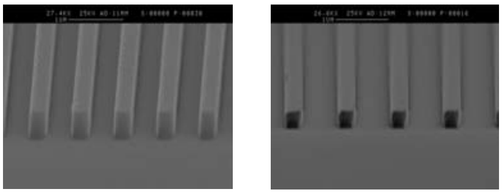

Figure 4. Descum of polystyrene pattern on quartz. CD constant at 350 nm before (left) and after (right) descum. The parameters were O_2 flow rate 10 sccm, Pressure 1 mTorr, ICP 600 W, RIE bias 10 W, He backside 10 Torr, Electrode -10°C, Time 2 min to remove 200 nm residual.

Nanoscale substrate etch

The requirements to the final substrate etch depend on the application and so are much more diverse than the stamp etch and descum. Examples are given of two ICP silicon etch processes with complementary attributes for nanoscale etching [7]. The first is a room temperature process using a C_4F_8-SF_6 gas mixture (Figure 5). The second is the cryogenic process using a SF_6-O_2 gas mixture (Figure 6). Control of silicon etched profile by means of the ICP process parameters is shown.

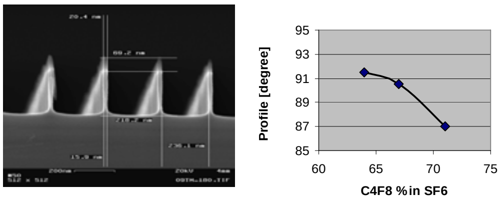

Fig.5 16nm Si lines etched by C_4F_8-SF_6 ICP process. Profile control by C_4F_8% (right)

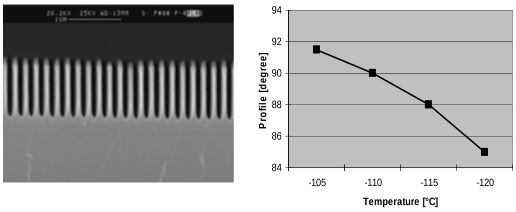

Figure 6. 1µm deep Si lines with 10:1 aspect ratio etched by ICP cryo process
Profile control by temperature (right)

Conclusions

The use of ICP for the three etching steps in a typical NIL process scheme has been demonstrated. The ICP etch shows superior capabilities regarding etching of high performance NIL stamps with well controlled profiles. The stable low pressure descum process possible with ICP effectively removes the residual polymer after imprinting with minimal loss of CD and ICP is also perfect for transferring the imprinted pattern into fused silica and silicon.

References

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